netX 90



- First Industrial Ethernet node in 10x10 mm² with two ARM[®] Cortex[®]-M4 processor cores, on-chip Flash, analog/mixed signal, and integrated PHYs
- Fulfills the highest demand on flexibility, determinism, and performance in terms of multiprotocol capability and low latency for short cycle times
- Enables developers to implement a profound secure by design concept compliant to the IEC 62443 series for industrial automation security
- Improves the application design of high-reliable systems with built-in diagnostics and enhanced data integrity for IIoT-enabled services



With the advent of Industrial IoT, as key technology for cyber-physical systems, Hilscher developed the next generation of network controllers, which builds on the success of the netX 51/52, where security is a core product value. The first member of this new family is the netX 90, which enables higher degrees of integration with enhanced performances and improved power efficiency ratings, suitable for industrial application designs with smaller form factors.

The increasing complexity of System-on-Chips (SoC), coupled with high software development and maintenance costs, associated with multiprotocol capabilities for real-time industrial communications, turned into market requests that promote solution-oriented concepts. Thus, the netX 90 accelerates this transition by providing a unique value proposition with emphasis on the interplay between hardware and software to improve time to markets.

Accordingly, the advanced SoC design brings together two separate system paradigms in one tiny package, i.e. one for real-time industrial communications and one for industrial applications. The inter-CPU data exchange between both systems, based on a consistent and uniform API, enables application developers to use the software protocol stack for communication tasks as loadable firmware (LFW), fully tested and pre-certified by Hilscher.

The conceptual LFW based software solution is independently usable whether the netX 90 is designed in as standalone chip application or as companion chip with host interface that fully carries out the real-time communication tasks for Industrial Ethernet or Fieldbus. The external host interface ensures a high degree of interoperability for maximum I/O data throughput with precise synchronization derived from the network cycle time.

In conclusion, the netX 90 provides a superior solution with an unmatched flexibility for a variety of industrial slave/ device applications for the process and factory automation.



netX 90 - Industrial Communication SoC



Built-in security

- Hardware support for cryptographic operations and security functions used by SSL/TLS services for protocols such as HTTPS, MQTT, and OPC UA
- Mask ROM Code assured secure boot levels with EMSA-PSS verifications that reject unauthorized firmware for secure software update procedures
- ▶ FIPS 140-2 compliant built-in cryptographic algorithms for highest encryption with different key lengths of up to RSA-4096, ECC-512, and AES-256

Highly integrated

- ▶ Two ARM[®] Cortex[®]-M4 high-performance processor cores, each with 125 DMIPS, to separate the communication tasks from the application tasks
- Integrated DC/DC converter, with on-chip BOD and POR circuits, for a 3.3V single-supply to simplify and optimize hardware application designs
- Notable BOM cost savings due to integrated Fast Ethernet PHYs, analog/mixed signal IPs, and efficient amounts of on-chip Flash and SRAM

Built-in diagnostics

- Enables the application design of high-reliable systems with built-in diagnostics and enhanced data integrity for IIoT-enabled cloud services
- Includes features such as power watch, clock supervisor, and fully ECC equipped on-chip memory for a high product reliability and robustness
- Provides a range of on-chip functions for voltage monitoring, time stamping, and die temperature sensing, applicable for predictive maintenance

Rich peripheral set

- Enhanced functional feature set with industry related on-chip peripherals such as 2x EnDat, 2x BiSS, 2x SSI, 8x IO-Link, 2x CAN, and 3rd MAC
- Rich set of standard peripherals for connectivity to interface sensor-specific ICs or submodules with fast I/O processing for electronic controls
- Integrated LVDSPHYs, which provide a low-cost backplane bus solution, for two primary use cases that enable unheard application designs

Interface Interface VDS| PHY netX 90 Dual-ported memory xC0xC1 10 mm x 10 mm 144-pin BGA SPI0-3 CPU CPU xPIC 100 MHz xPIC 100 MHz -TCM 8 KI GPIO0-3/T stack as consistent and uniform API -ТСМ 8 КВ ARM Cortex-M4 ARM Cortex-M4 FPU Memory 100 MHz 100 MHz nized with the network cycle time Flash 024 KB E iDPM RAM 576 KB EC MLED0-7 prototype in hours, not weeks System / Timer System / Timer Shared ROM 96 KB TPIU Memory Flash BOD RAM DC/DC 64 KB EC(Host Interface SQI XIP RC-OSC 2x ADC0-Communication Application BD-NX90-V6

Unmatched flexibility

- Flexible, programmable dual-channel xC subsystem, with switch and IEEE 1588 functionality, for all popular Industrial Ethernet and Fieldbus protocols
- Ensures a sustainable platform that flexibly adapts to emerging standards and future network requirements such as TSN, CC-Link IE Field Basic, etc.
- Supports the PROFINET IO Device specification V2.3 with the High Performance Profile for Conformance Class C and Network Load Class III

DC UA

DeviceNet

PROFI BOST

MQT

PROFO NET





CANOPER

Sercos



Ether**CAT**

ETHERNET

POWERLINK



- Industry-standard Eclipse based IDE
- Ready to use examples with NXHX boards
- Integrated utility tools and debugging support





- Overlaid structured software layout with DPM channel access functions to the industrial communication protocol
- High-speed access from either the external host interface or the internal host application, precisely clock synchro-
 - Ease of use, fast and hassle-free protocol stack implementation that enables application developers to set up a



Technical Data / Product Overview

	SoC	netX 90		
	Features	Communication	Application	
	ARM [®] Processor	Cortex®-M4 at 100 MHz with MPU	Cortex [®] -M4 at 100 MHz with MPU and FPU	
	Hilscher 32-bit RISC	xPIC at 100 MHz with 2x 8 KB TCM	xPIC at 100 MHz with 2x 8 KB TCM	
	SRAM (ECC)	576 KB	64 KB	
	Flash (ECC)	1024 KB	512 KB	
	Mask ROM	96 KB	-	
	DMA Controller	3 channels	3 channels	
	WDC (ARM / xPIC)	1/1	1/1	
	Timer (ARM / xPIC)	2x 32-bit / 3x 32-bit	2x 32-bit / 3x 32-bit	
	Built-in Bootloader	Host Interface (DPM/SPM), Ethernet (xC ₀ DHCP/TFTP), Serial (FTDI USB to JTAG/UART)		
	xC Subsystem	2 channels	-	
	IEEE 1588 SysTime	2	1	
	Fast Ethernet PHY	Dual-port, FX support	-	
	100 Mbps LVDSPHY	Dual-port	-	
	Ethernet MAC	10 / 100 Mbps, MII		
	UART (Up to 10 Mbaud)	1	2	
	SPI (Up to 50 MHz)	-	4	
	I ² C (Up to 3.4 MHz)	2	2	
	CAN (2.0B, SJA1000)	-	2	
	IO-Link V1.1 Controller	-	8 channels	
	MLED (PWM tuned)	4	8	
	PIO / GPIO / MMIO	-/4/-	Up to 49 / 8 / 16	
	Timer (PWM, IC/OC)	4x 32-bit (Min. 10 ns)	8x 32-bit (Min. 10 ns)	
ce Signal	ADC SAR (12-bit, 2 Msps)	2x 2 channels		
	EnDat 2.2 (Master E6)	-	2 (With RTM)	
	BiSS / SSI (Master MB)	-	2/2	
	Parallel (DPM)	8/16-bit (Read access min. 55 ns)	Internal 32-bit	
erfa	Serial (SPM)	2x SPI/QSPI (Up to 125 MHz/33 MHz)	-	
lute	MAC (PHY Mode)	MII (10/100 Mbps)	-	
Ž	SRAM / NOR / NAND / SDRAM	✓ / ✓ / - / ✓ (8/16-bit)		
Ĕ	SD/MMC / SDIO	SPI Mode / -		
ž	SQI (XIP)	1	XiP/Read only	
	Crypto Core	SSL/TLS accelerator, up to RSA-4096, ECC-512, AES-256, and SHA-512		
	Secure Boot	Mask ROM Code, EMSA-PSS		
	Built-in support	Security levels, AHB Firewall		
	CoreSight [™] ETM	JTAG/SWD, 4-bit TPIU		
	Boundary Scan	JTAG		
	DC/DC / POR / BOD	$\sqrt{ \sqrt{ } }$		
	Thermal diode	\checkmark		
	Clock Supervisor	Xtal (RC-Osc)		
	Power Supply	Single 3.3V		
	Temperature range	T _a -40°C +85°C		
	Power consumption	TBD		
	Package dimension	144-pin BGA, 10x10 mm ² , 0.8 mm Ball Pitch		

Note: Technical data may be changed without further notice

ev	Article Description	Article Number	Article
Overvie	NETX 90	2270.000	netX 90 Network Controller * Engineering Sample 2017 (Evaluation Board) / Mass Production 2018 * Please contact your local sales representative for further information

Headquarters

Network Sytsem Memory Core

Peripheral

Electrical Analog Debug Security External Host Mixed

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